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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,038	09/24/2003	Frankie F. Roohparvar	400.021US02	5054

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,038	ROOHPARVAR ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No._____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/8/05 have been fully considered but they are not persuasive.

In regards to applicants arguments that the references cited teach protection from writing and not protection from erasing: Since, in computers erasing is the same as writing 0 or random data (See any of Microsoft Press Computer Dictionary second edition Definition of Erase, PN 4,745,579 to Mead et al that teaches an Erase procedure, or PN 4,905,063 to Beltram et al that teaches that a write of 0 is an erase, or PN 5,140,182 to Ichimura that teaches to erase it is required to write a 0, or alternatively PN 5,173,876 to Kawashima et al that teaches that even for EEPROM's that require a different voltage to erase than write that to erase still requires writing a 0.) Chuang et al which teaches write protection inherently teaches erase protection since writing 0 or random data is required to erase.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang et al PN 6,031,757 in view of James, Jr. et al PN 6,240,519.

In regards to claims 1, 5: Chuang et al teaches a method for writing data to a first boot area (sector, including a "boot block" Column 1 lines 28-56) of a synchronous memory array device (Flash memory 11), the method comprising: initiating a write operation (write cycle or erase operation Column 4 lines 48-59 and Abstract) to the first boot area; reading data from a register circuit (32) and detecting a security voltage (V_{HH} or alternatively V_{IH}); and authorizing the write operation to the first boot area if the data is in a first state (Lock bit = 0) or the security voltage exceeds a predetermined voltage ($V_{HH} > Vcc$ or alternatively $V_{IH} > V_{IL}$ See line 2 and line 5 of Table 2). Chuang teaches write protection to a plurality of sectors/blocks. Chuang does not teach a plurality of boot areas. James teaches a memory array separated into a plurality of blocks with two boot blocks (204 and 206). It would have been obvious to a person of ordinary skill in the art at the time of the invention to have a second boot block because this would have allowed for additional boot block size to add code such as a prompt for an administrative password (Column 5 lines 29-59).

In regards to claim 2: Chuang teaches checking a status of a detection circuit (22,23,30,31) if the data is in a second state; and authorizing the write operation to the first boot area based on an output of the detection circuit (output = 0).

In regards to claim 3: Chuang teaches the detection circuit monitors an externally provided signal applied to the memory device (RP and WP).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang et al PN 6,031,757 in view of James, Jr. et al PN 6,240,519 as applied to claim 1 above, and further in view of Kynett et al PN 5,249,158.

In regards to claim 4: Le teaches write protection of a boot area of a synchronous memory as described above. Le also teaches write protection of any selected region. Le does not teach the structure of the synchronous memory or that the boot area is top bootable or bottom bootable. Kynett et al teaches a synchronous memory in which both top booting and bottom booting are supported (Column 8 lines 43-65). It would have been obvious to have Le's synchronous memory include both top booting and bottom booting because this would have allowed for greater system compatibility.

5. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang et al PN 6,031,757 in view of James, Jr. et al PN 6,240,519 as applied to claim 1 above and further in view of Johnson et al PN 5,343,437.

In regards to claim 6-9: Chuang in view of James teaches the write protection of a boot area of a synchronous memory as described above. Chuang in view of James however does not expressly teach the Lock bits being transferred to volatile memory upon system power up. Johnson et al teaches copying data from a non-volatile memory to a volatile memory upon system power up. It would have been obvious to copy the Lock bits to a volatile memory from the non-volatile memory upon power up because the volatile memories are faster than non-volatile memories.

In regards to claim 10: James inherently teaches data is stored in a second boot area of the plurality of boot areas when the first boot area no longer has sufficient capacity to hold additional data (See column 5 lines 28-59).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
January 27, 2006

PAUL R. MYERS
PRIMARY EXAMINER